REMARKS

By this amendment, claims 5, 6, 12, 13, 15 and 19 have been canceled, and claim 16 has been amended. Thus, claims 1-4, 7-11, 14, 16-18 remain pending. Favorable reconsideration of this application, as presently amended, and in light of the following discussion, is respectfully requested.

Allowable Subject Matter

Applicants wish to thank the Examiner for indicating in item 15 that claims 2, 4, 7, 9, 11 and 14 are allowed, and in item 16 that claims 16 and 18 contain allowable subject matter.

Claims 1 and 3 are rejected under 35 U.S.C. §102(e) as being anticipated by *Ker, et al.* (U.S. Patent No. 6,566,715, hereinafter "*Ker '715*").

Applicants respectfully traverse the above rejections and submit that the outstanding Action has misinterpreted the prior art in applying *Ker '715* to claim 1, for the following reason. Item 3 of the outstanding Action reads "... a fourth region 40 of the first conductivity type is disposed between the second region of said first MOS transistor and the third region of said second MOS transistor ...". And immediately prior it is stated that the second region of the first MOS transistor forms a source of the first MOS transistor, and the third region forms a source of the second MOS transistor. Hence, the Examiner is taking region 40 of *Ker '715* to be situated between the source of the first MOS transistor and the source of the second MOS transistor.

Applicants respectfully submit that this interpretation is in error, as stated in *Ker '715*'s description of Fig. 5A, in column 4, line 20: "Two n+ doped regions 36, functioning as the drain (electrode) of the substrate-triggered NMOS, are positioned between poly-silicon gates 34 on

the surface of the p-well 32. Between the n+doped regions 36, a p+ doped region 40 is positioned for the electrical connection to p-well 32 and serves as the trigger node for the substrate-triggered NMOS." From this description it is clear that *Ker '715*'s region 40 is situated between the drains, not the sources, as in the present application. Hence, *Ker '715*'s Fig. 5A does not disclose the subject matter of present claim 1.

Since *Ker '715* does not disclose the semiconductor structure of claim 1, it also does not disclose the structure of claim 3, which contains all of the limitations of claim1.

Claim 1 is rejected under 35 U.S.C. §102(e) as being anticipated by *Lee, et al.*, U.S. Patent No. 6,097,066 (hereinafter "*Lee*").

Lee is directed to an electro-static discharge protection structure for semiconductor devices which includes a plurality of first ring shape structure formed on a semiconductor wafer to act as the gates of the MOS devices. The areas in the inner side of the first ring shape structures are drain regions. A plurality of sources regions having second ring shape structures are formed around each sides the first ring shape structures.

Applicants respectfully traverse the above rejection and submit that the outstanding Action has misapplied the prior art in applying *Lee* to claim1, for the following reason. Both Figure 6 of *Lee*, and item 4 of the outstanding Action, describe the fourth region 550 as being disposed between drains 510, not between sources, as in the present application. Hence, *Lee*'s Figure 6 does not appear to disclose the semiconductor structure set forth in claim 1.

Claim 5 is rejected under 35 U.S.C. §102(e) as being anticipated by *Hsu et al.*, U.S. Patent No. 6,057,579 (hereinafter "*Hsu*").

Claim 5 has been canceled, hence the rejection thereto is now moot.

Claims 8 and 10 are rejected under §102(e) as being anticipated by *Ker '715*.

Applicants respectfully traverse the above rejections and submit that the outstanding Action has misinterpreted the prior art in applying *Ker '715* to claim 8, for the following reason. Item 6 of the outstanding Action reads "... A third N+ region 36 within said within said substrate for forming a source of a second MOS transistor ... wherein a p+ region 40 is disposed between the second N+ region of said first MOS transistor and the third N+ region of the second MOS transistor ...".

Hence, the outstanding Action is assuming region 36 to be a source. Applicants submit that this is in error, as stated in *Ker '715*'s description of Fig. 5A, in column 4, line 20: "Two n+ doped regions 36, functioning as the drain (electrode) of the substrate-triggered NMOS, ... Hence, *Ker '715*'s Fig. 5A does not disclose the subject matter of present claim 8.

Since *Ker '715* does not disclose the semiconductor structure of claim 8, it also does not disclose that of claim 10, which contains all of the limitations of claim 8.

Claim 8 is rejected under 35 U.S.C. §102(e) as being anticipated by *Lee*.

Applicants respectfully traverse the above rejection and submit that the outstanding Action has misapplied the prior art in applying *Lee* to claim 8, for the following reason. Both Figure 5 of *Lee*, and item 7 of the outstanding Action, describe the P+ region 550 as being

disposed between drains 510, not between sources, as in the present application. Hence, *Lee*'s Figure 5 does not disclose the semiconductor structure set forth in claim 8.

Claim 12 is rejected under 35 U.S.C. §102(e) as being anticipated by *Ker, et al.* USPN 6,072,219 (herein after "*Ker '219*").

As claim 12 has been canceled, the rejection thereto is now moot.

Claim 15 is rejected under 35 U.S.C. §102(e) as being anticipated by *Lin et al*, USPN 6,559,508 (hereinafter "*Lin*").

As claim 15 has been canceled, the rejection thereto is now moot.

Claim 17 is rejected under 35 U.S.C. §102(e) as being anticipated by *Lin*.

Applicants respectfully traverse the above rejection and submit that the outstanding Action is misapplying the prior art in applying *Lin* to claim 17, for the following reason. The outstanding Action has not identified where in *Lin* the purported third and fourth MOSFETs of second conductivity type are disclosed. Without such an indication, Applicants respectfully maintain that the semiconductor structure of claim 17 is not disclosed in *Lin*.

Claim 19 is rejected under 35 U.S.C. §102(e) as being anticipated by *Lin, Ker,* and *Lee,* and also *Maria Verhaege et al.,* US PG-Pub 2002/0033507.

As claim 19 has been canceled, the rejection thereto is now moot.

Claim 12 is rejected under 35 U.S.C. §103(a) as being unpatentable over *Hsu*.

As claim 12 has been canceled, the rejection thereto is now moot.

Claims 6 and 13 are rejected under 35 U.S.C. §103(a) as being unpatentable over *Hsu,* in view of *Admitted Prior Art (hereinafter "APA").*

As claims 6 and 13 have been canceled, the rejections thereto are now moot.

In view of the amendments to the claims and the remarks set forth above distinguishing the claimed invention from the cited prior art references, Applicants submit that the Examiner's objections and rejections have been overcome. It is therefore respectfully requested that the Examiner withdraw the objections and rejections and allow the present claims.

If, for any reason, it is felt that this application is not now in condition for allowance, the Examiner is requested to contact Applicants' undersigned attorney at the telephone number indicated below to arrange for an interview to expedite the disposition of this case.

In the event that this paper is not timely filed, Applicants respectfully petition for an appropriate extension of time. The fees for such an extension or any other fees which may be due with respect to this paper, may be charged to Deposit Account No. 50-2394.

Respectfully submitted,

IPS, Inc.

Robert J. Forsell, Jr.
Reg. No. 51,693

Customer No. **34003**
5717 Colfax Avenue
Alexandria, VA 22311
Tel: (703) 379-9625
Fax: (703) 379-9628
RJF/km